REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on May 13, 2008 and the references cited therewith.

Applicants have amended claims 1 and 8. Applicants have not added or canceled any claims. Applicants previously canceled claims 14-20. Accordingly, claims 1-13 remain pending in the application, of which claims 1 and 8 are independent. Support for the amendments to claims 1 and 8 is found, at least, for example, on page 18, line 24 – page 19, line 7.

Claim Rejections – 35 U.S.C. § 112

In the Office Action, claims 1-13 were rejected under 35 U.S.C. § 112, first paragraph and second paragraph as, respectively, lacking enablement and being indefinite. Both of these rejections are based on the aspects of claims 1-13 referencing "a state transition diagram." Without conceding the merits of the rejections, Applicants note that independent claims 1 and 8 have been amended to remove the references to a state transition diagram. Therefore, the rejections of independent claims 1 and 8, and their respective dependent claims 2-7 and 9-13 are moot. Applicants respectfully request that the rejections be withdrawn.

Claim Rejections - 35 U.S.C. § 103

In the Office Action, claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,613,114 to Anderson et al. (hereafter "Anderson") in view of U.S., Patent 5,163,016 to Har'El et al. (hereafter "Har'El"), and alternatively over Anderson in view of U.S. Patent 6.041,176 to Shiell. Applicants respectfully traverse this rejection.

Claim 1, as amended, recites:

> A method of performing a context switch operation, the method comprising:
>
> setting an index register on an address portion of a state machine in a peripheral system to a first index value by a host computer, the first index value indicating a first register to be accessed;
>
> ***in response to setting the index register to the first index value, accessing context data in the first register of the peripheral system based upon the first index value***;
>
> setting the index register to a second index value by the host computer, the second index value indicating a second register to be accessed; and
>
> ***in response to setting the index register to the second index value, accessing context data in the second register of the peripheral system based upon the second index value***, wherein the first and second registers are collocated with the peripheral system.

It is well settled that in order to establish a *prima facie* case of obviousness it must the shown that each and every element of the rejected claims is disclosed or described in the cited documents. Applicants respectfully submit that claim 1 is not obvious over Anderson, Har'El and Shiell, because these patents, alone or in combination, do not disclose or describe each and every element of the claim.

Claim 1 is directed to a method for performing a context switch operation. The method of claim 1 includes setting an index register on an address portion of a state machine to a first index value, where the first index value indicates a first register (e.g., context register). **In response to setting the index register to the first index value, claim 1 includes, accessing context data in the first register based on the first index value.** The method of claim 1 also includes setting the index register to a second index value, where the second index value indicates a second register. **In response to setting the index register to the second index value, claim 1 includes, accessing context data in the second register based on the second index value.** Anderson in combination with Har'El or Shiell does not disclose or describe such an approach.

Anderson discloses a current thread register 64, which, in the Office Action, is asserted as constituting the index register of claim 1. As disclosed in Anderson, the current thread register 64 is used to indicate a currently executing thread. *See* Anderson, column 8, lines 7-42. The value (i.e., current thread ID) of the current thread register 64 is retrieved by a custom context switching unit 76 under the direction of a thread scheduling unit. The custom context switching unit 76 decodes the current thread ID to determine the location of a corresponding thread object. Custom switch-out and switch-in routines are used to save and access context data under the direction of the thread scheduling unit 74, not in response to a value being written to the current thread ID register. *See* Anderson, col. 9. lines 17-56.

Accordingly, because Anderson disclose accessing context data under the direction of a thread scheduling unit 74 and does not access context data in response to an index value being written to an index register on an address portion of a state machine as recited in claim 1, Anderson fails to disclose at least this aspect of claim 1. Neither Har'El nor Shiell compensate for these deficiencies of Anderson and are not cited as such. Har'El and Shiell are cited as disclosing a state machine

Based on the foregoing, claim is not rendered obvious on Anderson in view of Har'El or in view of Shiell. Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-7 depend from claim 1 and include all of its limitations. Without addressing the merits of the remarks made in the Office Action with respect to claims 2-7, which are not conceded, Applicants respectfully submit that claims 2-7 are not obvious over Anderson in view of Har'El or in view of Shiell on the same basis as discussed above with respect to claim 1. Accordingly, Applicants respectfully request that the rejection of claims 2-7 be withdrawn.

Claim 8 is an apparatus claim that includes similar limitations as discussed above with respect to claim 1. Therefore, claim 8 and its dependent claims are not obvious over Anderson in view of Har'El or in view of Shiell on at least the same basis as claim 1. Thus, Applicants respectfully request that the rejection of claims 8-13 be withdrawn. Also, Applicants respectfully note that the remarks in the Office Action made with respect to claims 8-13 are not conceded.

Also in the Office Action, claims 1-13 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent 6,292,851 to Takeda in view of Har'El and, alternatively, over Takeda in view of Shiell. Applicants respectfully traverse this rejection.

As discussed above, claim 1 recites a method for performing a context switch operation. In the method of claim 1, context data is accessed in registers in response to setting index values corresponding with the registers in an index register. Takeda does not relate whatsoever to performing a context switch operation let alone disclose the elements of claim 1 as asserted in the Office Action.

The Abstract of Takeda is as follows:

> In a system having a supervisory module and at least one supervised module mounted on separate circuit cards in a common housing, the supervised module has a memory unit in which alarm and status information is stored by a processing unit, which gathers the alarm and status information from other integrated circuits in the supervised module. The supervisory module obtains the alarm and status information from the memory unit, without having to specify the physical addresses of integrated circuits and registers in the supervised module. The processing unit in the supervised module also makes register settings in the integrated circuits in the supervised module, on behalf of the supervisory module.

Applicants have examined Takeda and are unable to find any reference whatsoever to performing a context switch operation or accessing context data in registers in response to setting an index value in an index register. Takeda instead relates to the collection of alarms and status information in a supervised module and obtaining those alarms and status information in a supervisory module. While Takeda may disclose accessing information in a register, Takeda does not discuss or even mention accessing context data or performing a context switch operation as recited in claim 1.

Accordingly, because Takeda does not relate at all to context switch operations or accessing context data in response to setting an index value in an index register, Takeda fails to disclose at least these aspects of claim 1. Neither Har'El or Shiell compensate for these deficiencies of Takeda and are not cited as such. Har'El and Shiell are both cited for disclosing a state machine

Based on the foregoing, claim 1 is not rendered obvious on Takeda in view of Har'El or in view of Shiell. Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-7 depend from claim 1 and include all of its limitations. Without addressing the merits of the remarks made with respect to claims 2-7, which are not conceded, Applicants respectfully submit that claims 2-7 are not obvious over Takeda in view of Har'El or in view of Shiell on the same basis as discussed above with respect to claim 1. Accordingly, Applicants respectfully request that the rejection of claims 2-7 be withdrawn.

Claim 8 is an apparatus claim that includes similar limitations as discussed above with respect to claim 1. Therefore, claim 8 and its dependent claims are not obvious over Takeda in view of Har'El or in view of Shiell on at least the same basis as claim 1. Thus, Applicants respectfully request that the rejection of claims 8-13 be withdrawn. Also, Applicants respectfully note that the remarks in the Office Action made with respect to claims 8-13 are not conceded.

Double Patenting Rejection

In the Office Action, claims 1-13 were provisionally rejected on the grounds of nonstatutory obviousness-type double patenting, as being unpatentable over claims 1, 4-5 of copending application No. 11/314,036 in view of Maupin.

Respectfully, a terminal disclaimer will be timely filed in the later-allowed of the '036 application and the present application.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (360-930-3533) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

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Date September 15, 2008 By: /Paul W. Churilla – Reg. No. 47,495/
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